

# 915GV-M5A Rev: 1.1

## Schematics Version History Table :

Circuit Ver.	PCB Ver.	Total Page	Modified Page(s)	Date
A	A	36		08/03/' 04
B	B	36		09/01/' 04
C	C	36	28,29,33	09/20/' 04
D	D	36	25,26,27	09/21/' 04
1.0A	1.0A	36	10,22,24,25	10/12/' 04
1.0B	1.0B	36	15,22,24	11/07/' 04
				02/24/' 05
1.1	1.0B	36	29	03/31/' 05

## Page Title of Schematic :

Title	Page	Title	Page
Cover Sheet	1		
System Block Diagram	2		
P4 LGA775P Part A	3		
P4 LGA775P Part B	4		
P4 LGA775P Part C	5		
P4 LGA775P Part D	6		
P4 LGA775P Part E	7		
Clock Generator(CK410)	8		
I-GSD(MCH)Part A & E & F	9		
I-GSD(MCH)Part D	10		
I-GSD(MCH)Part B & C	11		
I-GSD(MCH)Part G	12		
DDIMM 1&2 ( DDR SDRAMs )	13		
DDIMM 3&4 ( DDR SDRAMs )	14		
DDR & V_FSB_VTT Power	15		
PCI EXPRESS 16-PORT	16		
ICH6 Part A & D (SATA-CONNECTOR)	17		
ICH6 Part B & C (RTC)	18		
ICH6 Part E & F (POWER & GND)	19		
IDE1 Connector	20		
USB/FWH	21		
LPC_FDD/KB/M	22		
I/O Ports	23		
H/W Monitor	24		
AC97 Codec	25		
Audio Interface	26		
ATX Power & Front Panel	27		
LAN	28		
Vcore DC-DC	29		
MIS DC-DC(DUAL & VDDQ)	30		
PCI Slot 1&2	31		
PCI Slot 3	32		
Back I/O	33		
VT6307 (1394)	34		
TPM (TRUSTED PF-MODELE)	35		
Schematic Change History	36		

DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	F/E/H/G	PREQ-2	PGNT-2
1394	20	D	PREQ-3	PGNT-3
LAN	21	E	PREQ-4	PGNT-4

PCB : 244 x 244 mm ; 4 layers

**INTEL  
P4 Processor  
PSC, Tejas -  
LGA 775 pin**

BW : 4.1GB/s @ FSB : 533MHz & Freq : 133MHz  
BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz

SIZE : Min 128MB (ONE 256Mb X 16 Single-Sided DEVICES)  
SIZE : Max 4GB (Four 512Mb X 8 Double-Sided DEVICES)  
BW : 8.5GB/s @ DDR2 : 400/533MHz  
BW : 6.4GB/s @ DDR : 333/400MHz

**INTEL  
i915GV  
1210pin FC-BGA**

**DDIMM1: DDR Socket 184P**

**DDIMM2 : DDR Socket 184P**

**DDIMM3: DDR Socket 184P**

**DDIMM4 : DDR Socket 184P**

**VGA (G only)**

Analog Display  
RAMDAC: 400MHz  
Resolutions Up To 2048x1536@75Hz

BW : 2GB/s (Support Lsoch)

**USB1 2 ports** **USB2 2 ports** **USB3 2 ports** **USB4 2 ports** **USBLAN 8 ports**

USB V2.0

**INTEL  
ICH6  
609pin EBGA**

**PCIEx1**

BW : 133MB/s @ Freq : 33MHz

**IDE1 40pin**

Up to Ultra ATA/100  
Two IDE Channel

**PCI1 Slot 120pin @ AD17**

**PCI2 Slot 120pin @ AD18**

**PCI3 Slot 120pin @ AD19**

**Line in**  
**Line out**  
**Mic in**  
**Center/Bass out**  
**Surround**  
**Side-Surround**

**Audio Codec  
ALC880**

AC' 97 & Lan I/F

LPC bus

**intel  
FWH  
32pin PLCC**

**Super I/O  
W38627THF  
128pin PQFP**

**TPM 1.1**

**SATA1 7Pin**  
**SATA2 7pin**  
**SATA3 7Pin**  
**SATA4 7pin**

BW : 150MB/s

**VIA 1394  
(OPTION)**

**10/100  
Lan**

**USBLAN  
RJ45**

**CONN/  
HEADER**

<b>ECS Elitegroup Computer Systems</b>			
Title <b>System Block Diagram</b>			
Size <b>B</b>	Document Number <b>915GV-M5A</b>	Rev <b>1.1</b>	
Date: <b>Monday, April 11, 2005</b>	Sheet <b>2</b>	of <b>36</b>	

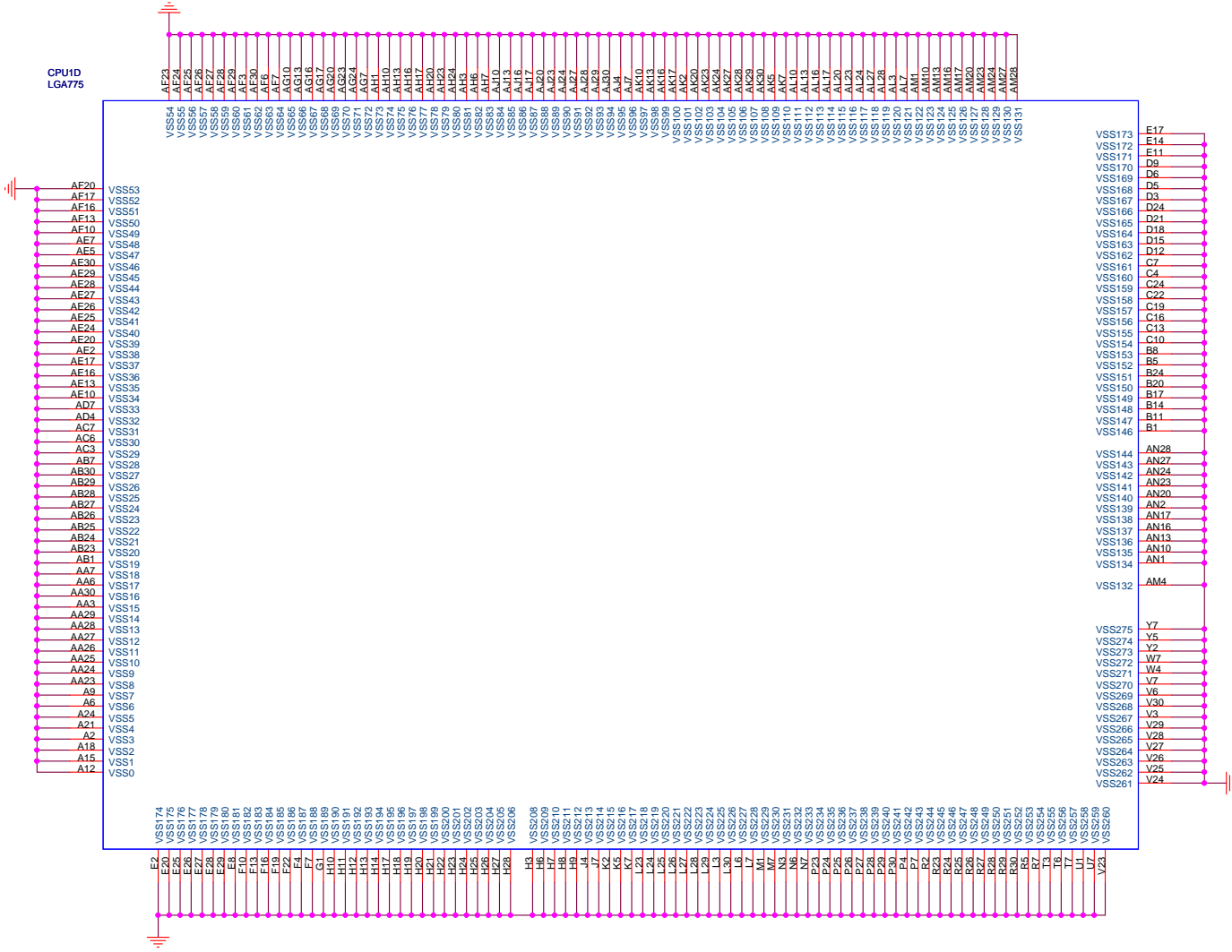


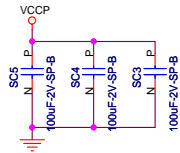
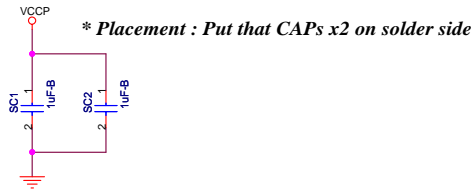
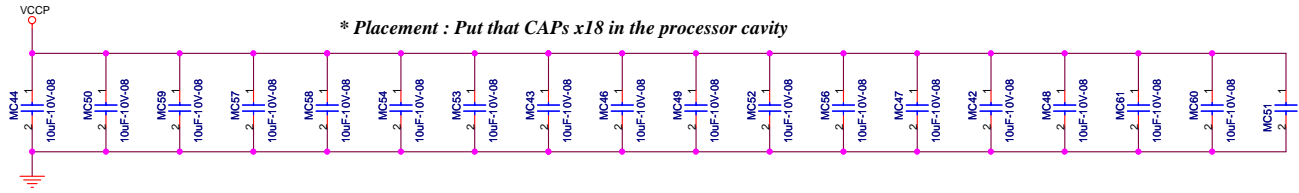




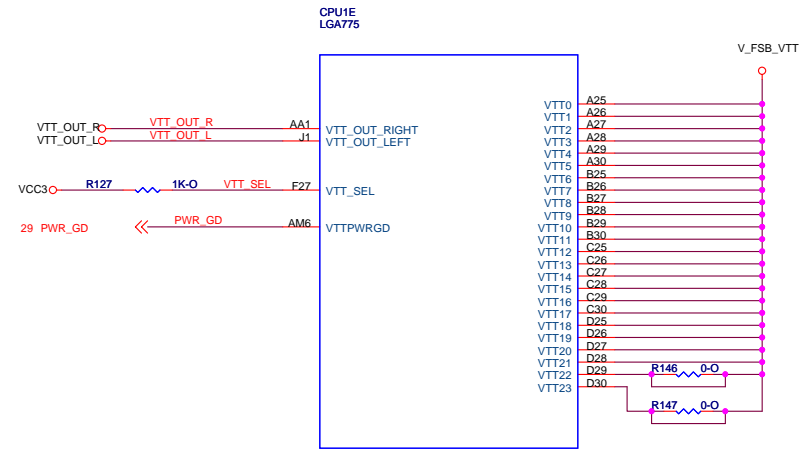
CPU1C  
LGA775

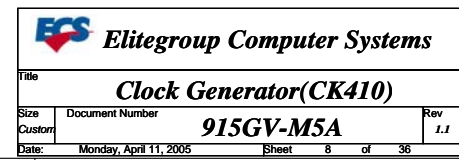
CPU1D  
LGA775





VTT\_SEL=0 for the Tejas processor







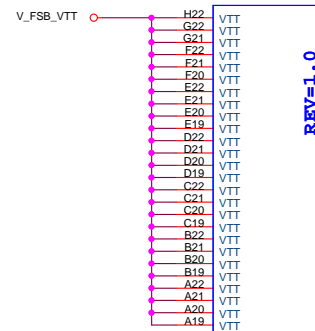
3 H D0	H D0	J33	HD0#	HA3#	H29	H A3	H A3	3
3 H D1	H D1	J34	HD1#	HA4#	H29	H A4	H A4	3
3 H D2	H D2	J35	HD2#	HA5#	H30	H A5	H A5	3
3 H D3	H D3	J36	HD3#	HA6#	H30	H A6	H A6	3
3 H D4	H D4	J37	HD4#	HA7#	H31	H A7	H A7	3
3 H D5	H D5	J38	HD5#	HA8#	H31	H A8	H A8	3
3 H D6	H D6	J39	HD6#	HA9#	H32	H A9	H A9	3
3 H D7	H D7	J40	HD7#	HA10#	H32	H A10	H A10	3
3 H D8	H D8	J41	HD8#	HA11#	H33	H A11	H A11	3
3 H D9	H D9	J42	HD9#	HA12#	H33	H A12	H A12	3
3 H D10	H D10	J43	HD10#	HA13#	H34	H A13	H A13	3
3 H D11	H D11	J44	HD11#	HA14#	H34	H A14	H A14	3
3 H D12	H D12	J45	HD12#	HA15#	H35	H A15	H A15	3
3 H D13	H D13	J46	HD13#	HA16#	H35	H A16	H A16	3
3 H D14	H D14	J47	HD14#	HA17#	H36	H A17	H A17	3
3 H D15	H D15	J48	HD15#	HA18#	H36	H A18	H A18	3
3 H D16	H D16	J49	HD16#	HA19#	H37	H A19	H A19	3
3 H D17	H D17	J50	HD17#	HA20#	H37	H A20	H A20	3
3 H D18	H D18	J51	HD18#	HA21#	H38	H A21	H A21	3
3 H D19	H D19	J52	HD19#	HA22#	H38	H A22	H A22	3
3 H D20	H D20	J53	HD20#	HA23#	H39	H A23	H A23	3
3 H D21	H D21	J54	HD21#	HA24#	H39	H A24	H A24	3
3 H D22	H D22	J55	HD22#	HA25#	H40	H A25	H A25	3
3 H D23	H D23	J56	HD23#	HA26#	H40	H A26	H A26	3
3 H D24	H D24	J57	HD24#	HA27#	H41	H A27	H A27	3
3 H D25	H D25	J58	HD25#	HA28#	H41	H A28	H A28	3
3 H D26	H D26	J59	HD26#	HA29#	H42	H A29	H A29	3
3 H D27	H D27	J60	HD27#	HA30#	H42	H A30	H A30	3
3 H D28	H D28	J61	HD28#	HA31#	H43	H A31	H A31	3
3 H D29	H D29	J62	HD29#					
3 H D30	H D30	J63	HD30#					
3 H D31	H D31	J64	HD31#					
3 H D32	H D32	J65	HD32#					
3 H D33	H D33	J66	HD33#					
3 H D34	H D34	J67	HD34#					
3 H D35	H D35	J68	HD35#					
3 H D36	H D36	J69	HD36#					
3 H D37	H D37	J70	HD37#					
3 H D38	H D38	J71	HD38#					
3 H D39	H D39	J72	HD39#					
3 H D40	H D40	J73	HD40#					
3 H D41	H D41	J74	HD41#					
3 H D42	H D42	J75	HD42#					
3 H D43	H D43	J76	HD43#					
3 H D44	H D44	J77	HD44#					
3 H D45	H D45	J78	HD45#					
3 H D46	H D46	J79	HD46#					
3 H D47	H D47	J80	HD47#					
3 H D48	H D48	J81	HD48#					
3 H D49	H D49	J82	HD49#					
3 H D50	H D50	J83	HD50#					
3 H D51	H D51	J84	HD51#					
3 H D52	H D52	J85	HD52#					
3 H D53	H D53	J86	HD53#					
3 H D54	H D54	J87	HD54#					
3 H D55	H D55	J88	HD55#					
3 H D56	H D56	J89	HD56#					
3 H D57	H D57	J90	HD57#					
3 H D58	H D58	J91	HD58#					
3 H D59	H D59	J92	HD59#					
3 H D60	H D60	J93	HD60#					
3 H D61	H D61	J94	HD61#					
3 H D62	H D62	J95	HD62#					
3 H D63	H D63	J96	HD63#					

GMCHA

REV=1.0

PSB

Grantsdale DDR1 MCH\_7

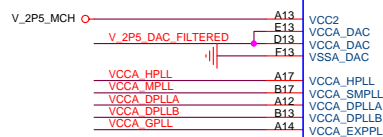


GMCHC

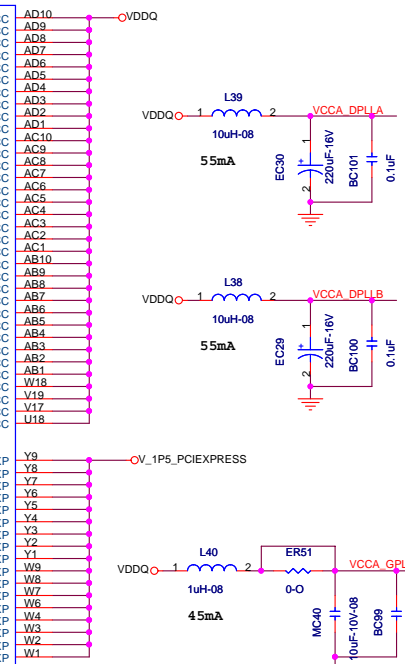
REV=1.0

POWER

DCR under 60mOhm



Grantsdale DDR1 MCH\_7



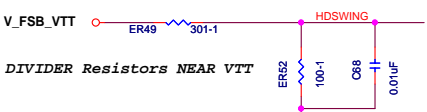
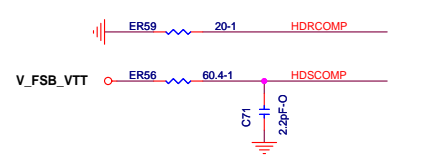
GMCHF

REV=1.0

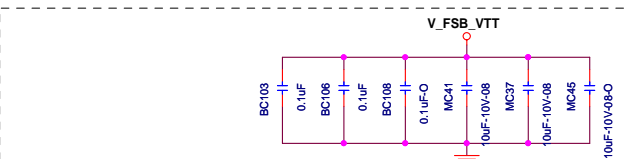
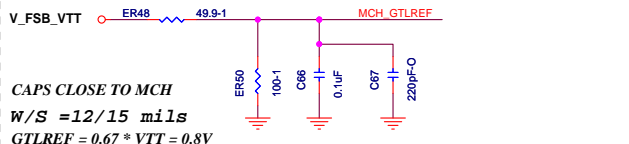
POWER & GND

Grantsdale DDR1 MCH\_7

BSEL TABLE	
2 1 0 PSB FREQUENCY	
0 0 1 133 MHZ (533)	
0 1 0 200 MHZ (800)	

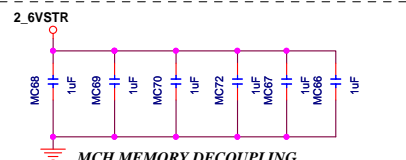


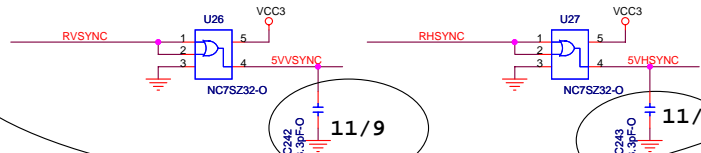
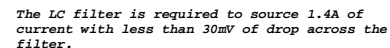
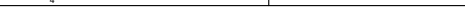
HDSWING W/S =10/7 mils  
HDSWING S/B (1/4\*VTT +/- 2%)

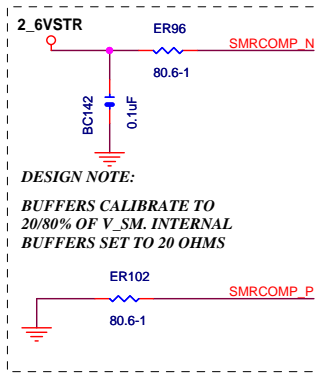


FSB GENERIC DECOUPLING

CAPS FOR FSB GENERIC

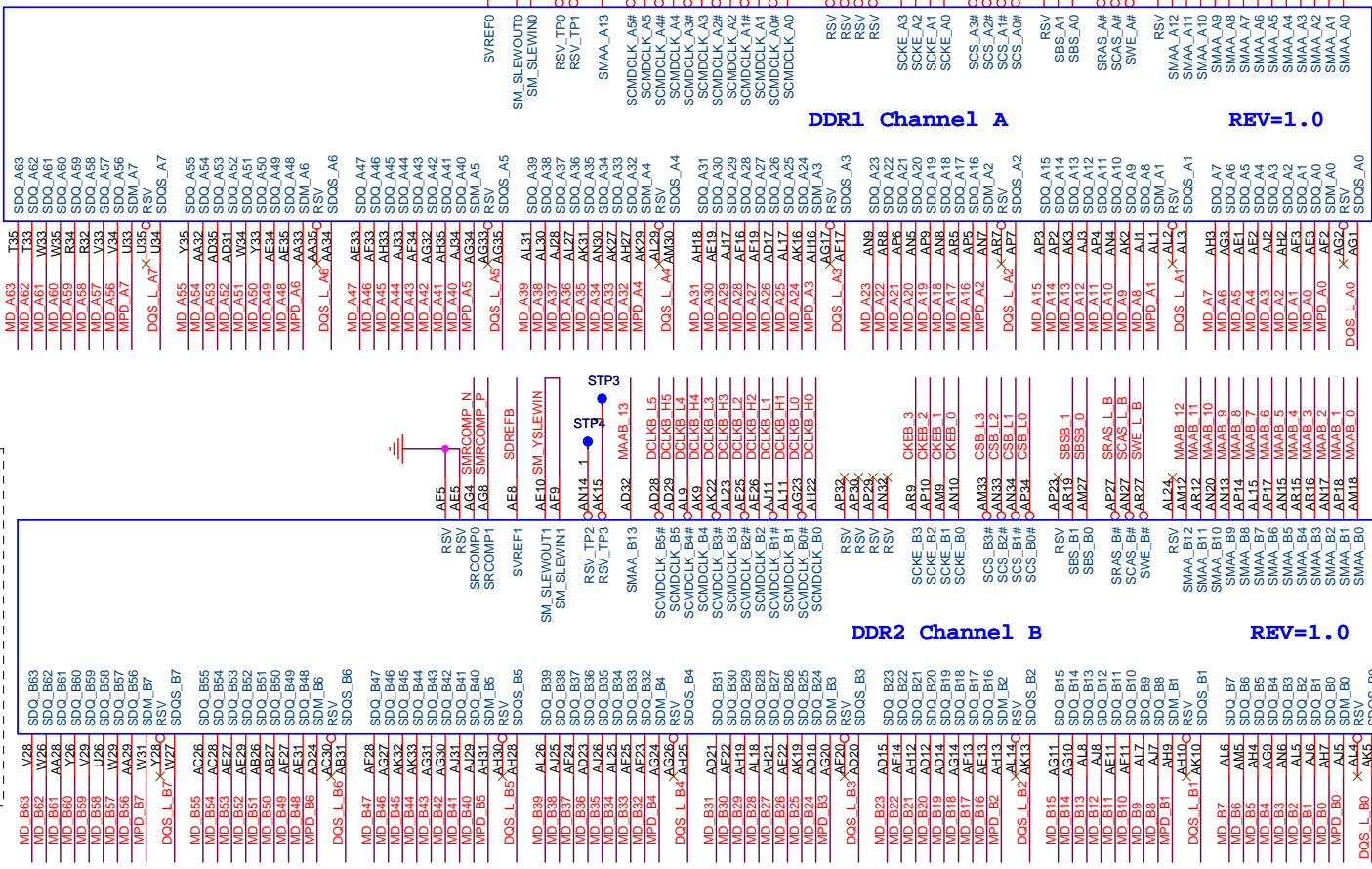







13	CSA_L[0..3]	<<	CSA_L[0..3]
14	CSB_L[0..3]	<<	CSB_L[0..3]
13	CKEA_L[0..3]	<<	CKEA_L[0..3]
14	CKEB_L[0..3]	<<	CKEB_L[0..3]
13	DCLKA_L[0..5]	<<	DCLKA_L[0..5]
13	DCLKA_H[0..5]	<<	DCLKA_H[0..5]

SWE_L_A	»	SWE_L_A	13
SCAS_L_A	»	SCAS_L_A	13
SRAS_L_A	»	SRAS_L_A	13
SWE_L_B	»	SWE_L_B	14
SCAS_L_B	»	SCAS_L_B	14
SRAS_L_B	»	SRAS_L_B	14
SBSA_0	»	SBSA_0	13
SBSA_1	»	SBSA_1	13
SBSB_0	»	SBSB_0	14
SBSB_1	»	SBSB_1	14



GMCHC  
Grantsdale DDR1 MCH\_7

 <b>Elitegroup Computer Systems</b>			
<b>Title</b> <b><i>I-GSD(MCH)Part B &amp; C</i></b>			
<b>Size</b> <b>B</b>	<b>Document Number</b> <b><i>915GV-M5A</i></b>		<b>Rev</b> <b><i>1.1</i></b>
<b>Date:</b> Monday, April 11, 2005		<b>Sheet</b> 11 <b>of</b> 36	


GMCHG

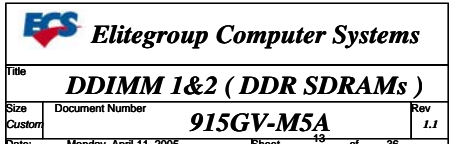
RSV

REV=1.0

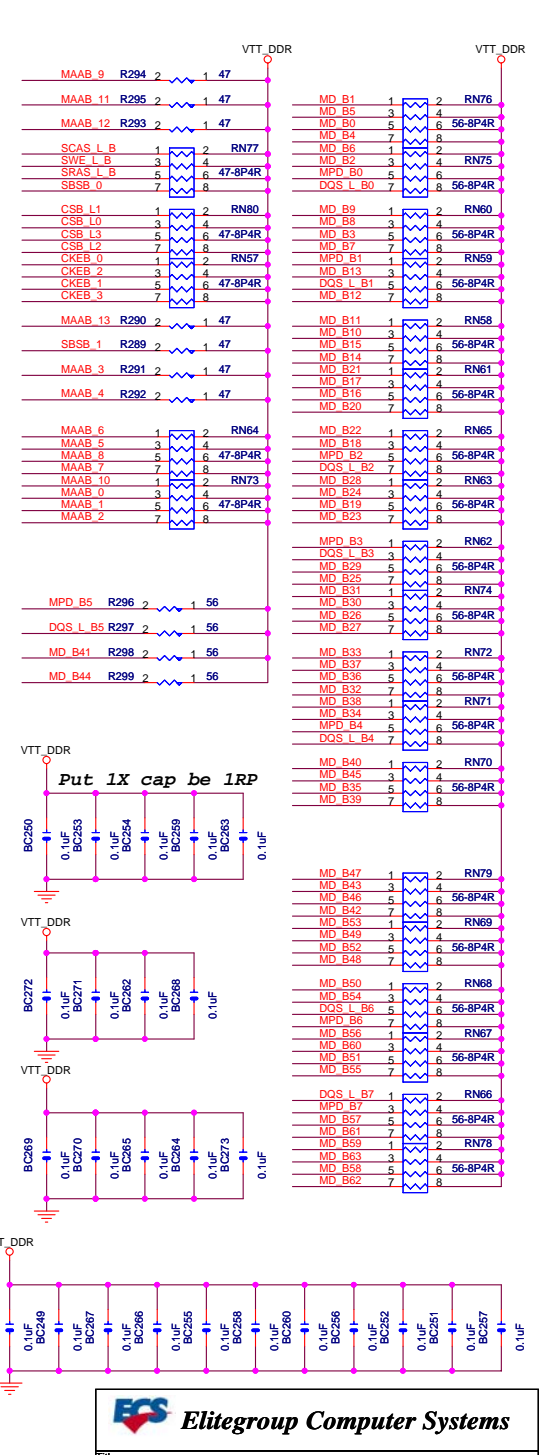
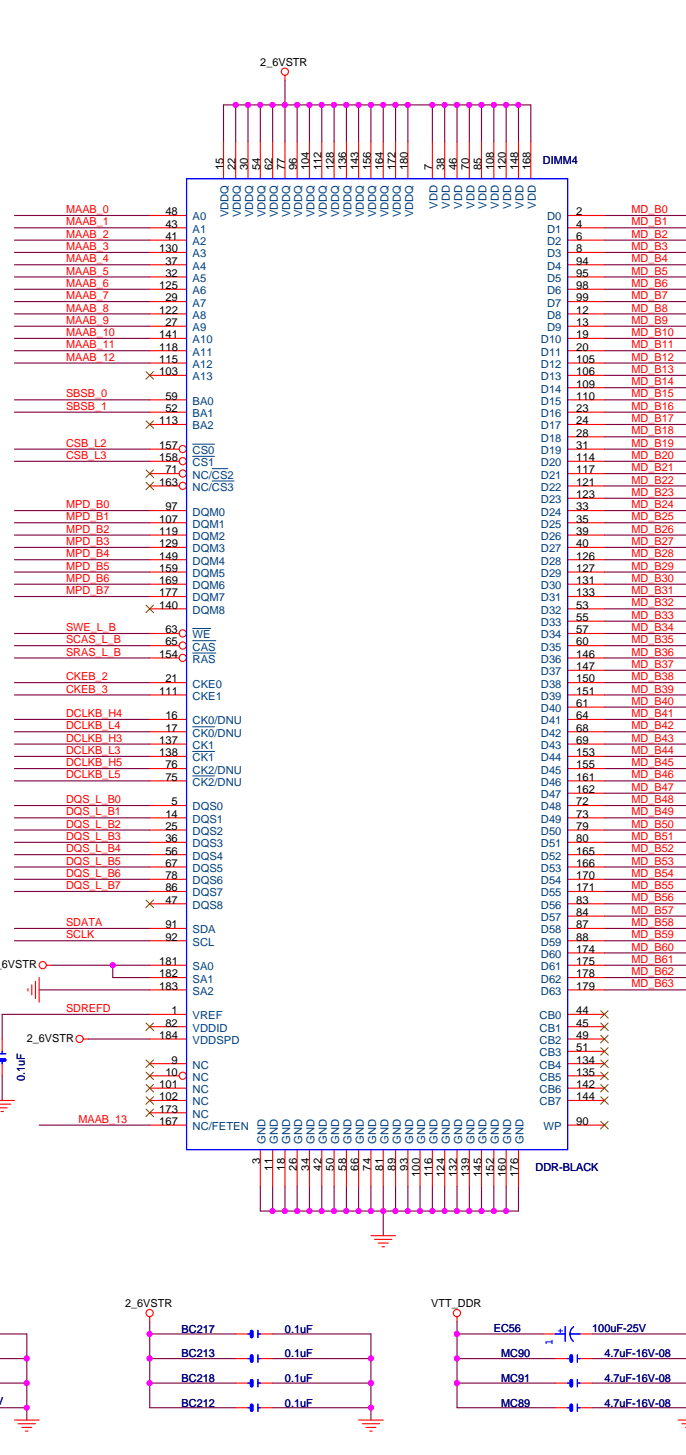
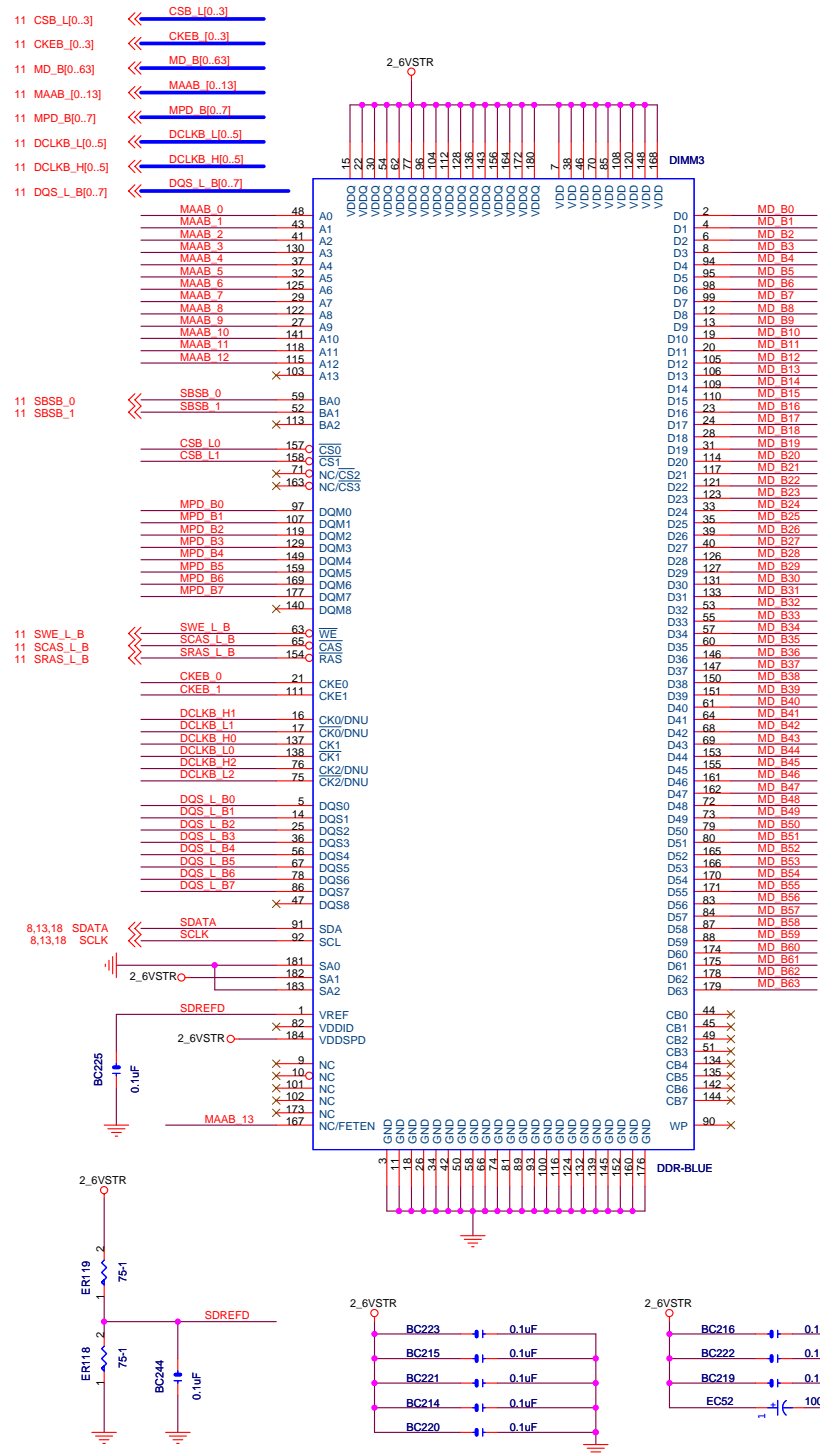
GND

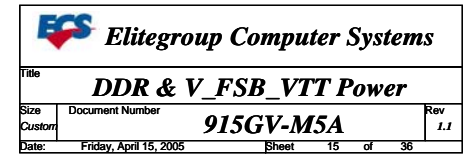
Grantsdale DDR1 MCH\_7

 Elitegroup Computer Systems			
Title			
Schematic Change History			
Size	Document Number	915GV-M5A	Rev
Custom			1.1
Date:	Monday, April 11, 2005	Sheet 12 of 36	



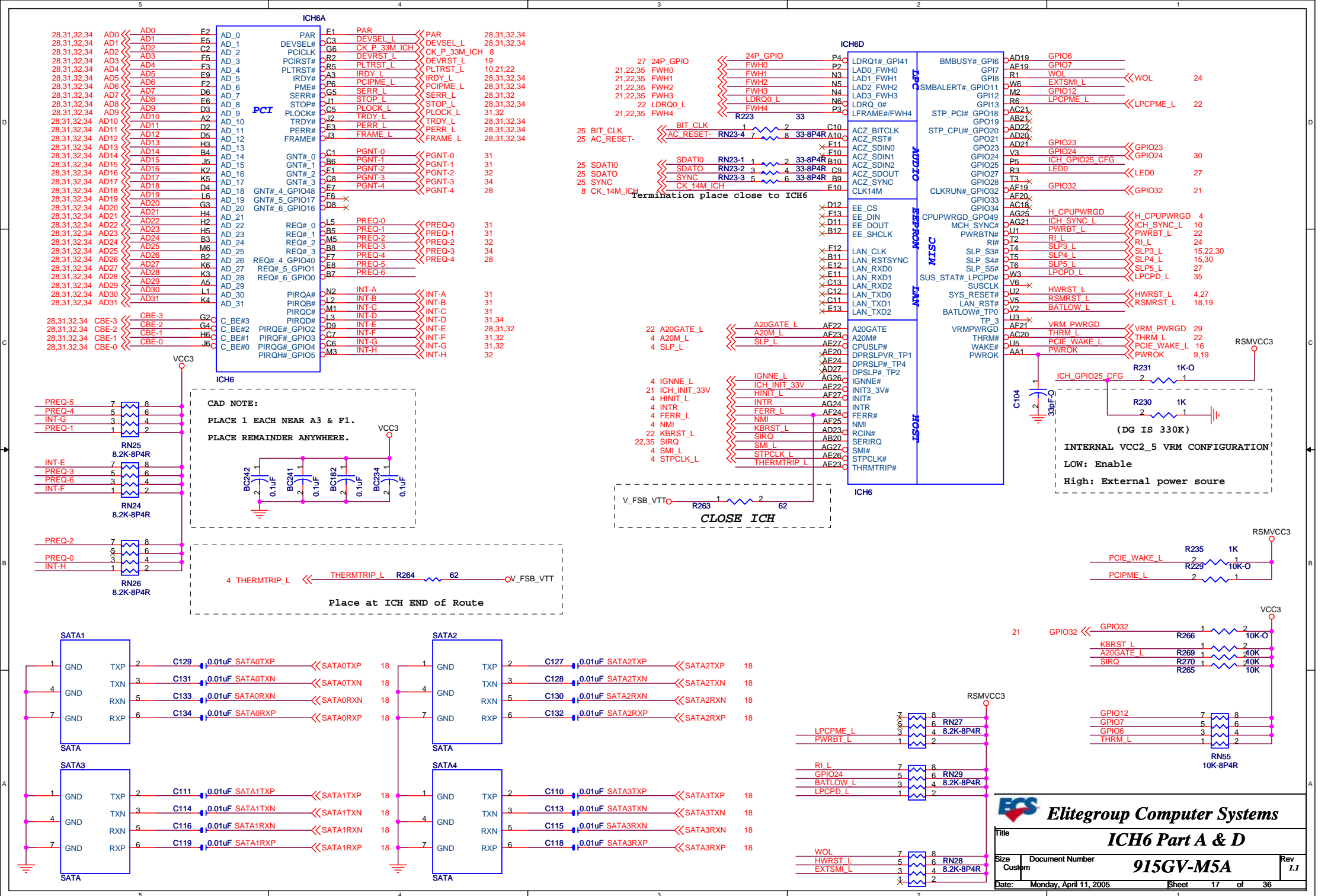


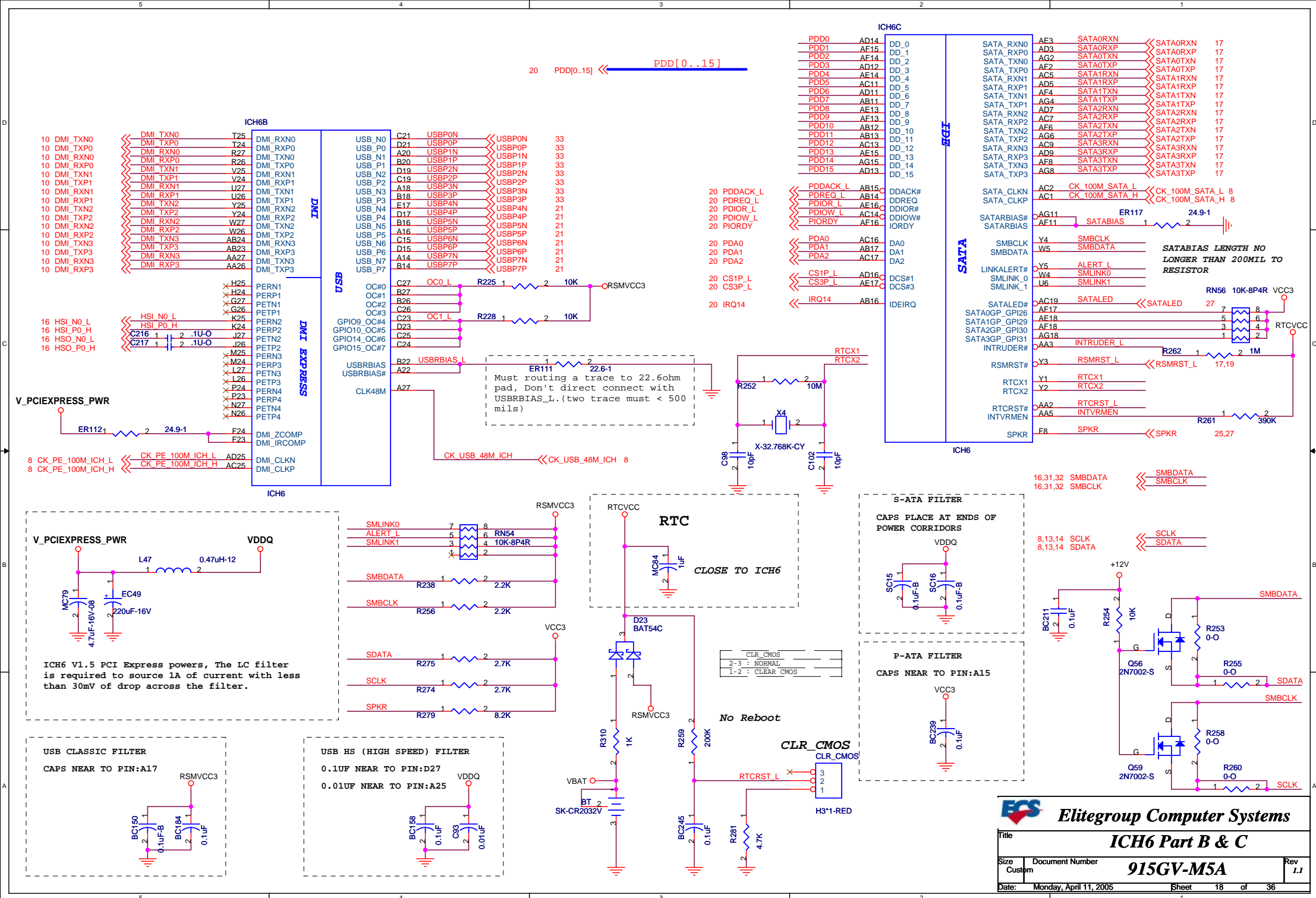


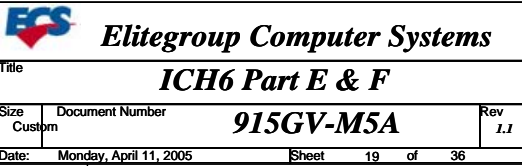


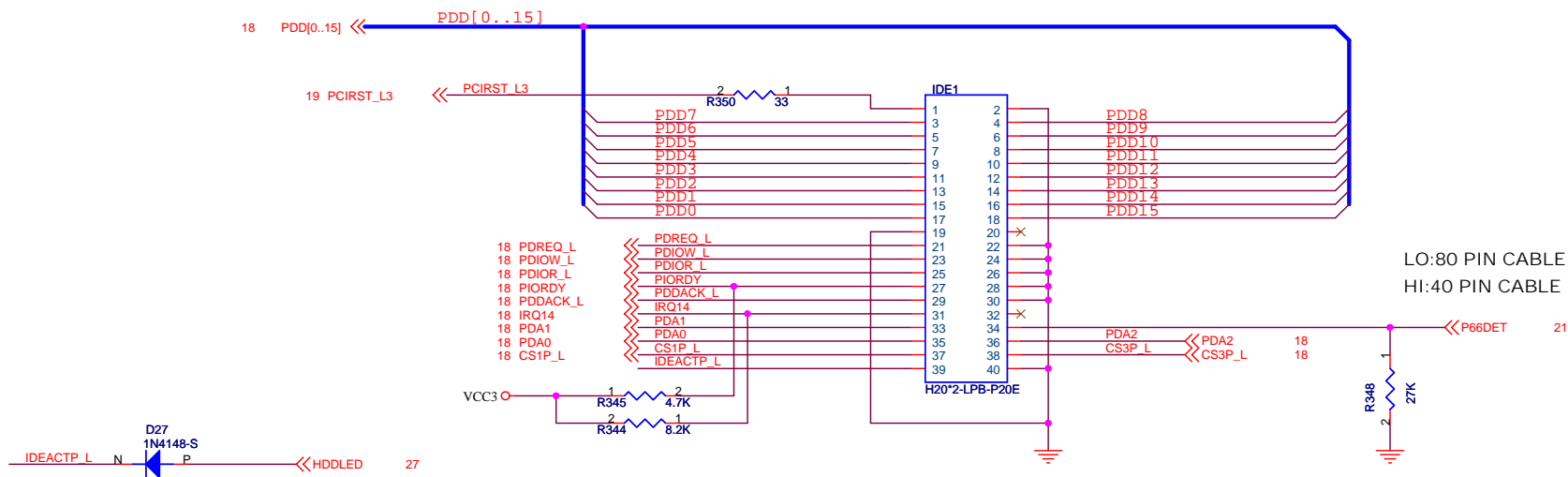






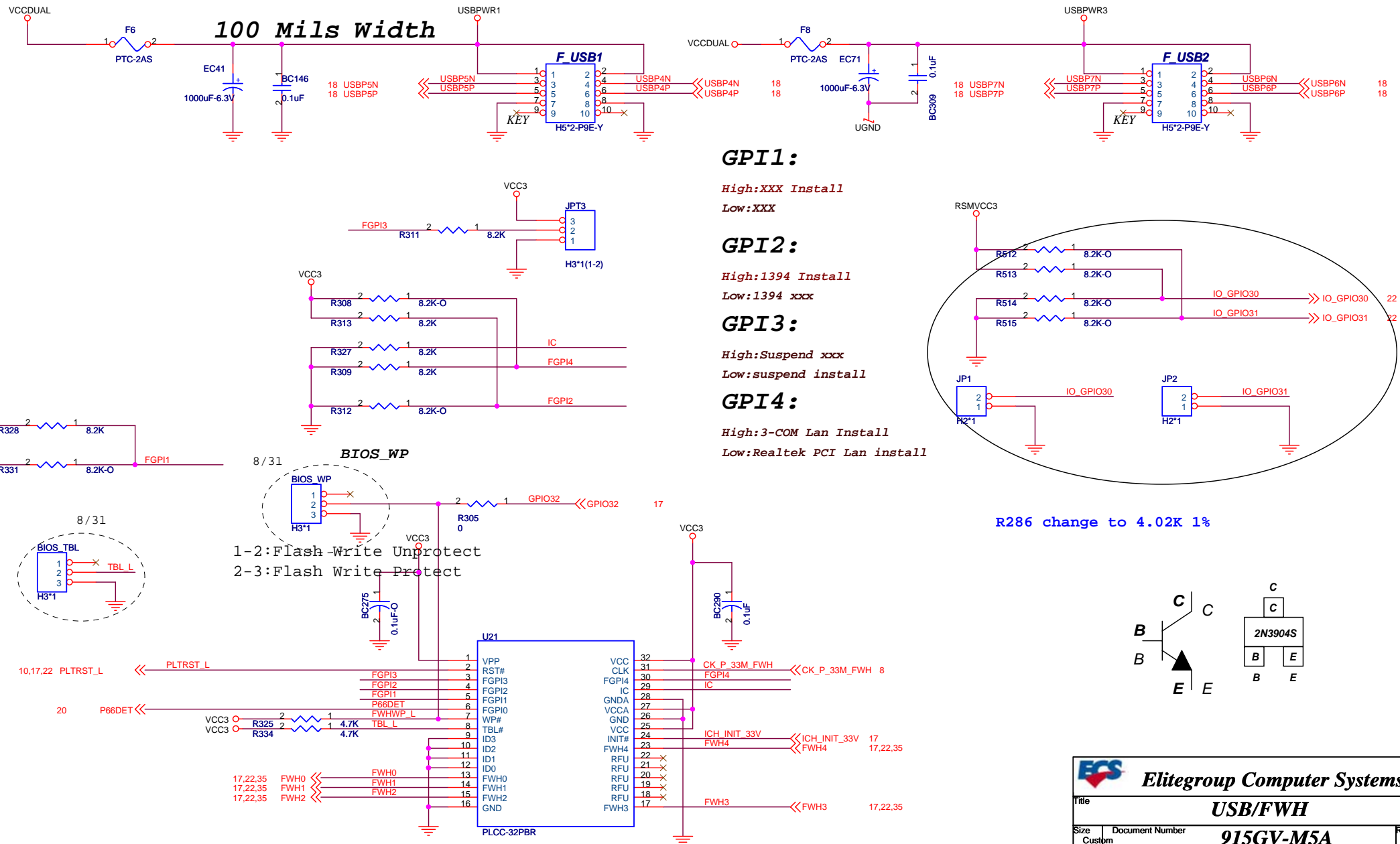


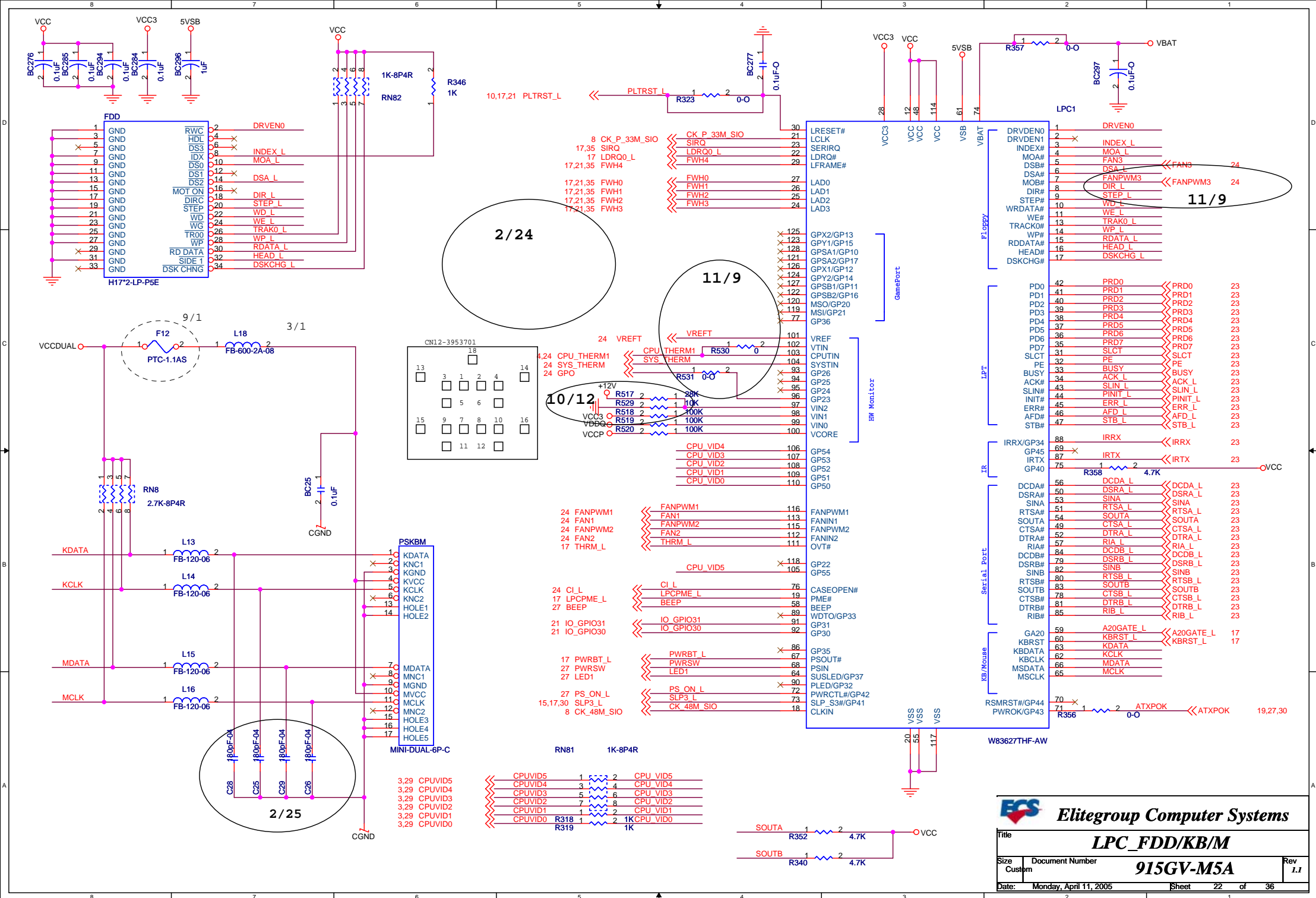




DATA LINES SHOULD BE MATCHED TO STROBES ( XDIOR\_L , XIORDY\_L) WITHIN +/- 250 MIL,  
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

# USB PORT INTERFACE



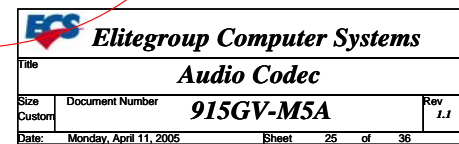
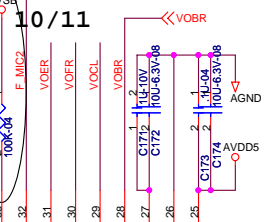
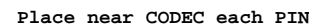
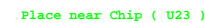
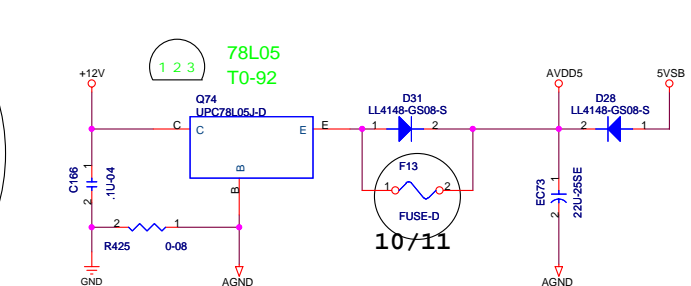




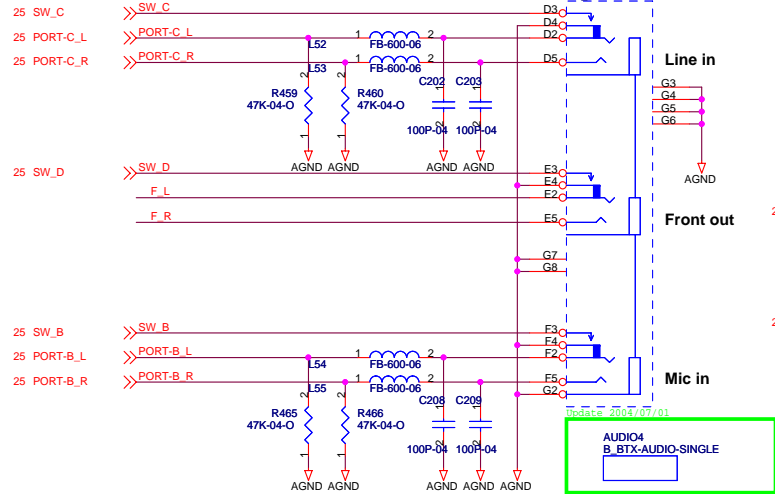




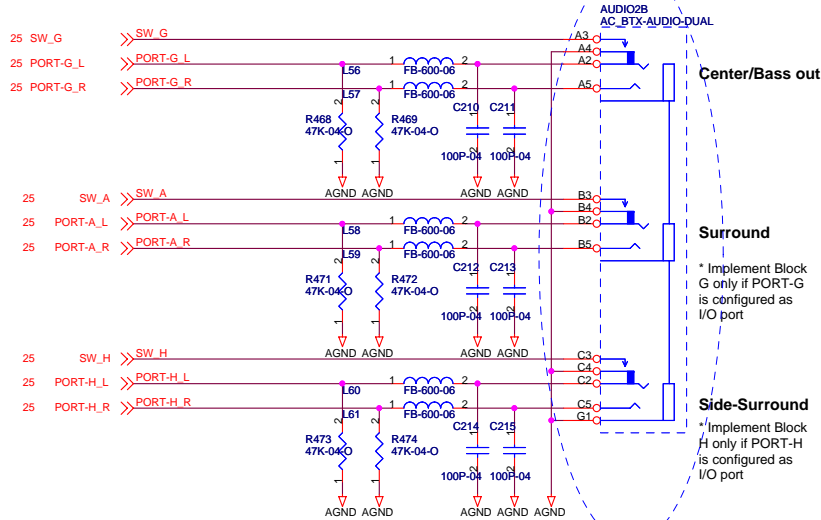




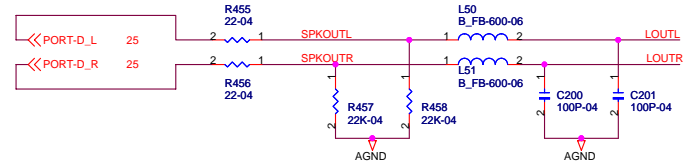
# Rear Panel Onboard Analog I/O



## Rear Panel (Optional Rear Audio Panel)

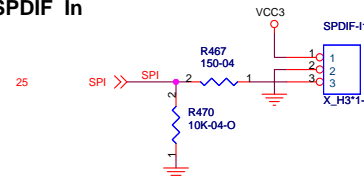


The schematic should consist with PINs define of I/O connector.

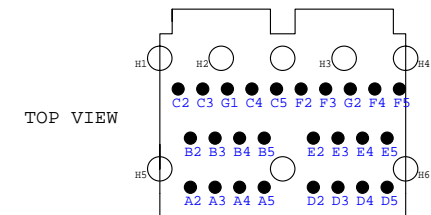
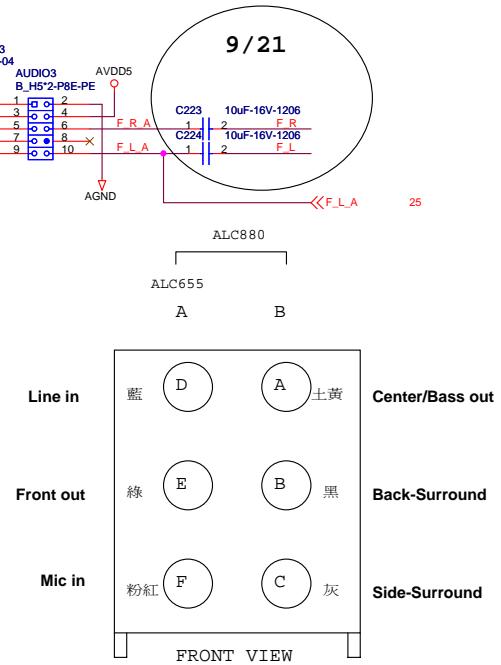
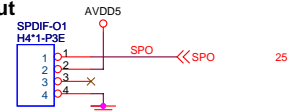


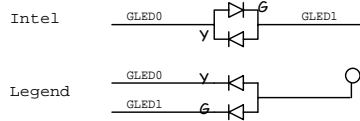
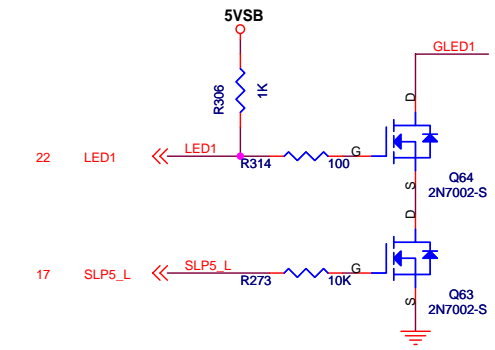
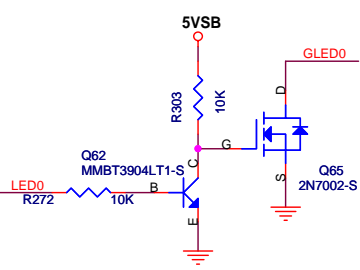
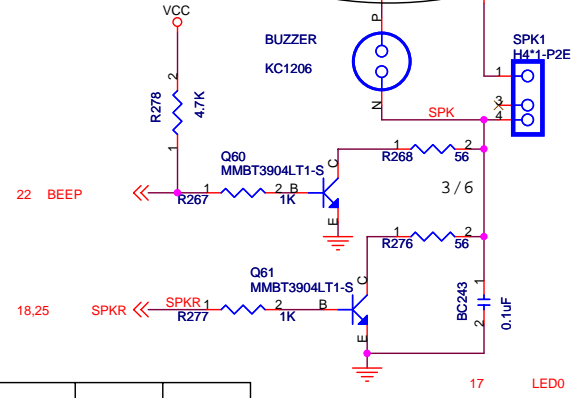
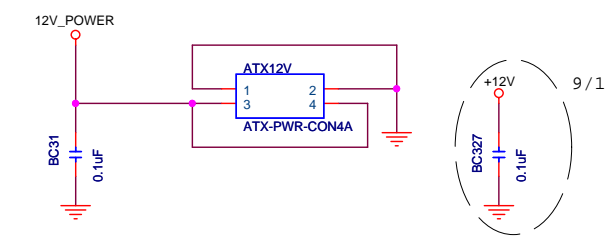
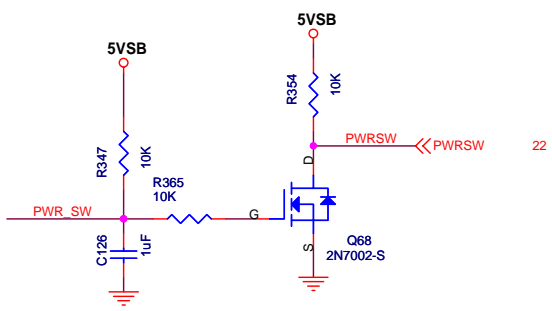
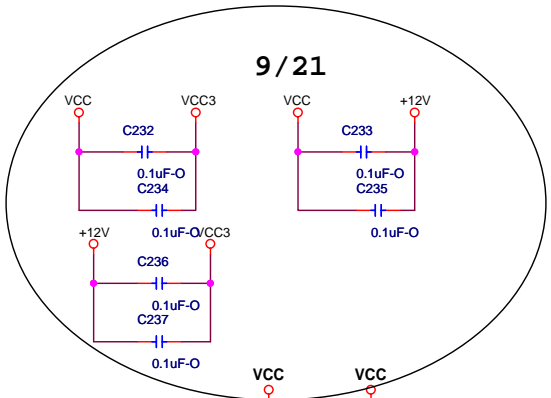
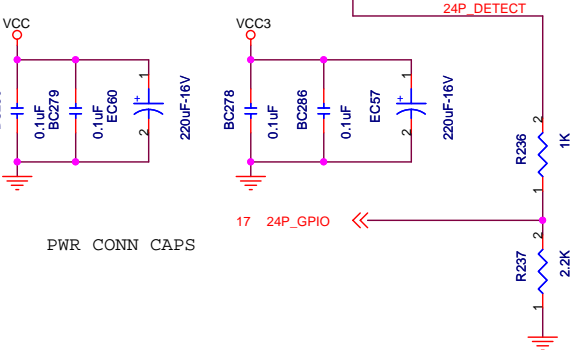
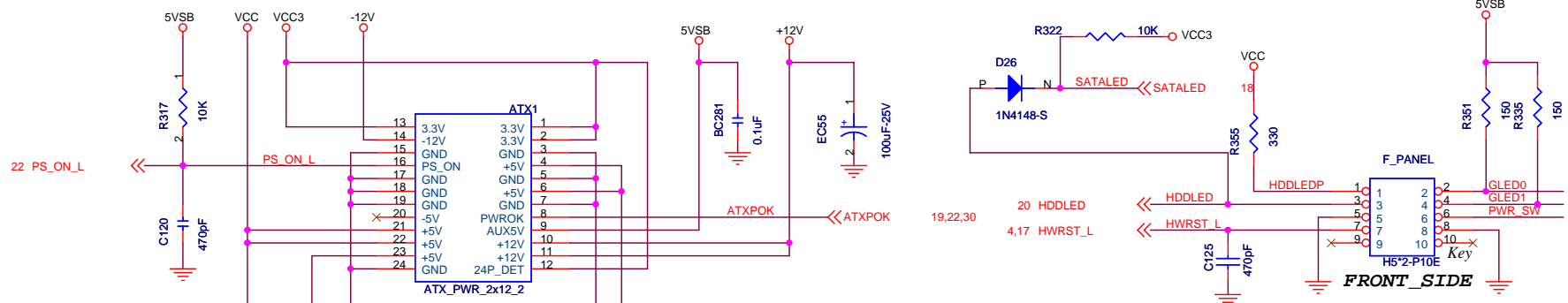
## SPDIF I/O

### SPDIF In

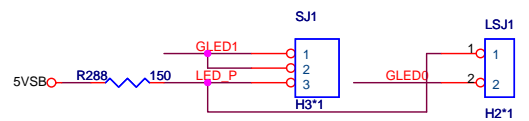
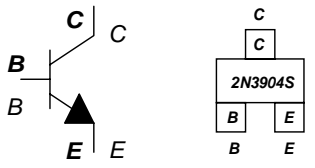


### SPDIF Out





	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking	Dark
LSJ1(1,2)	Dark	Dark	Light	Dark
SJ1(1,3)(2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH



**Elitegroup Computer Systems**

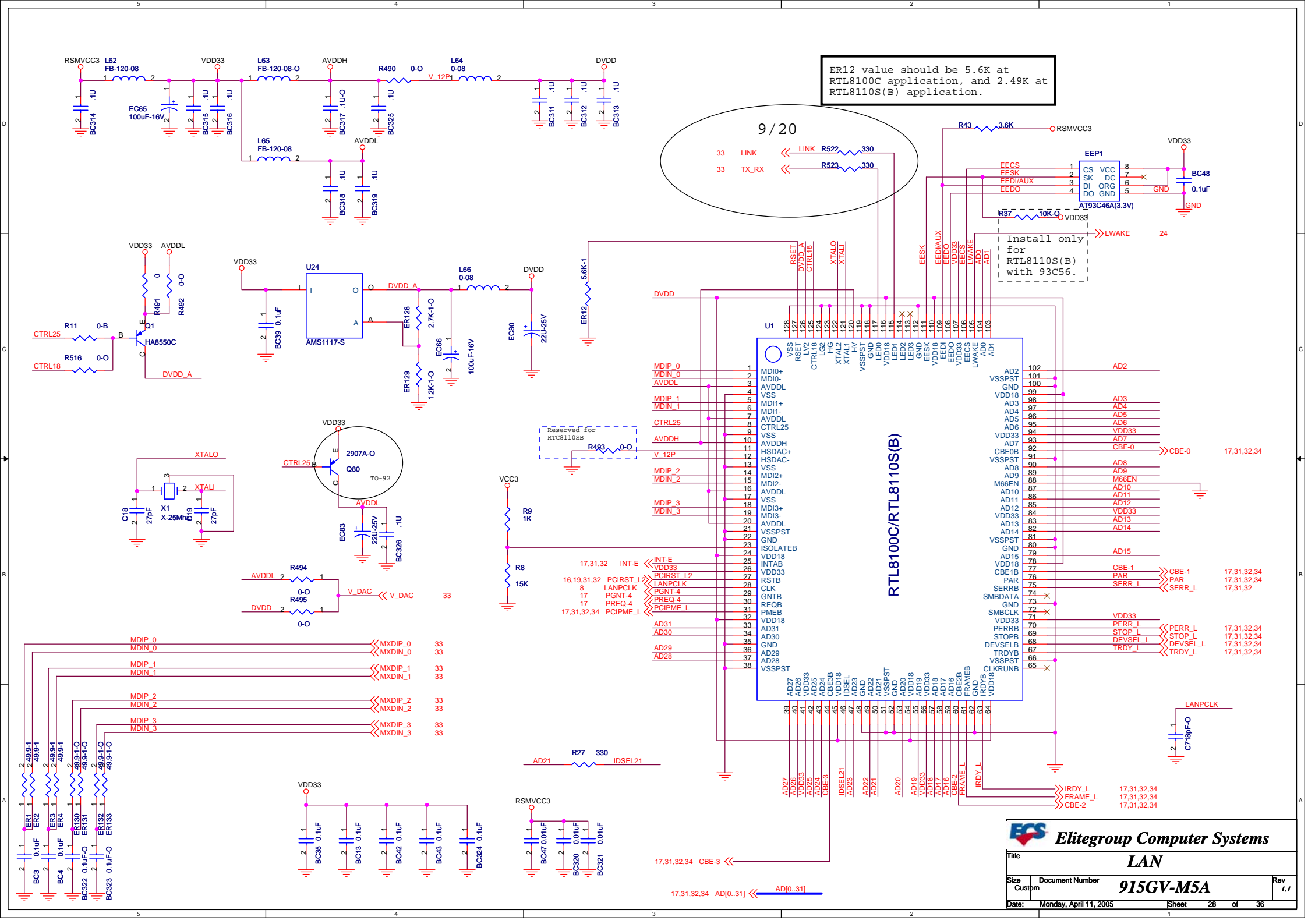
**ATX Power & Front Panel**

**915GV-M5A**

Date: Monday, April 11, 2005

Sheet 27 of 36

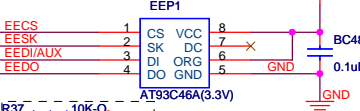
Rev 1.1



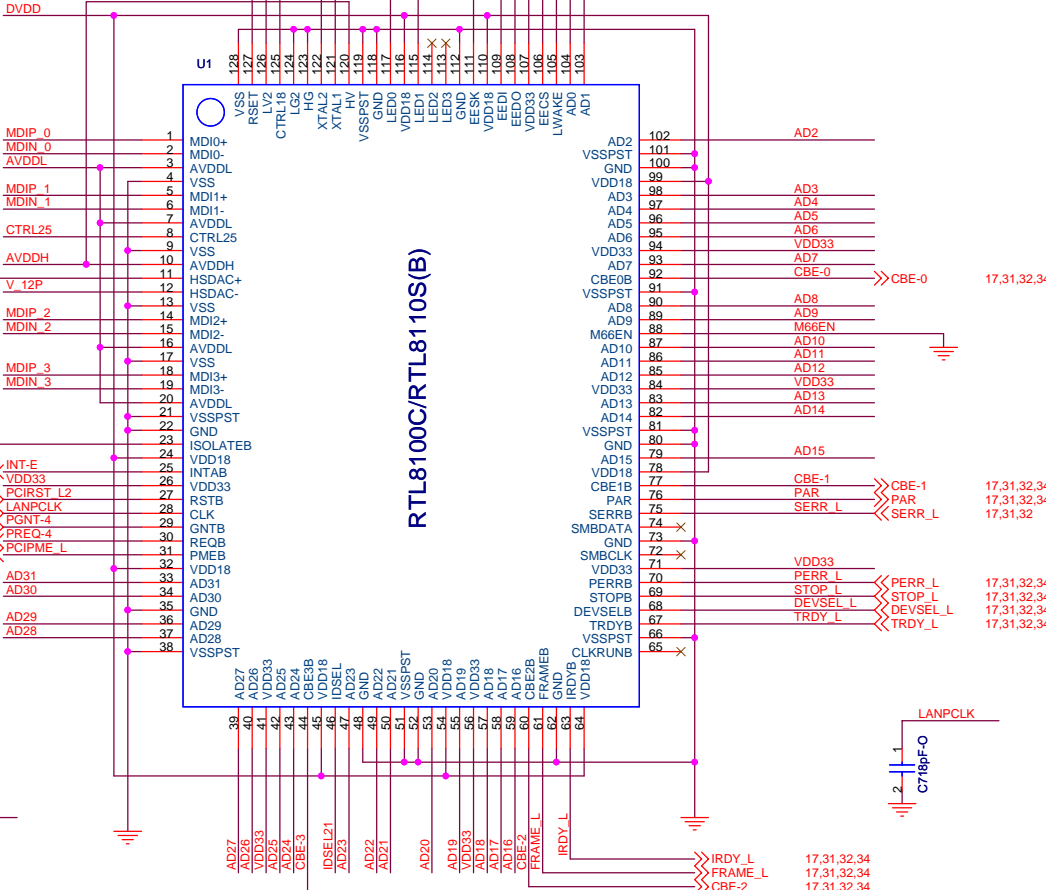
ER12 value should be 5.6K at  
RTL8100C application, and 2.49K at  
RTL810S(B) application.

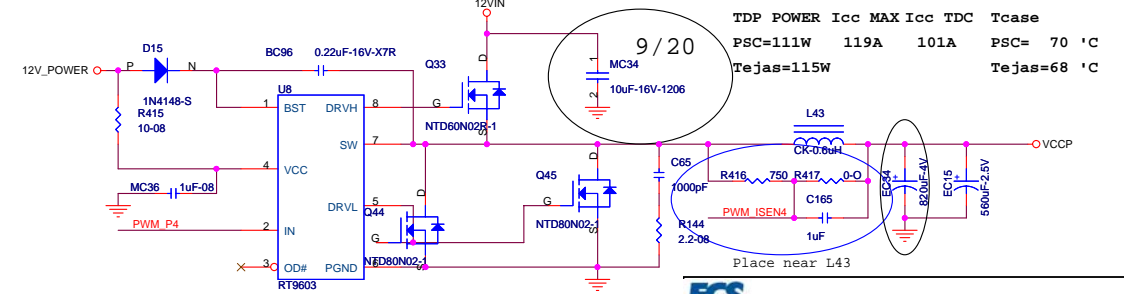
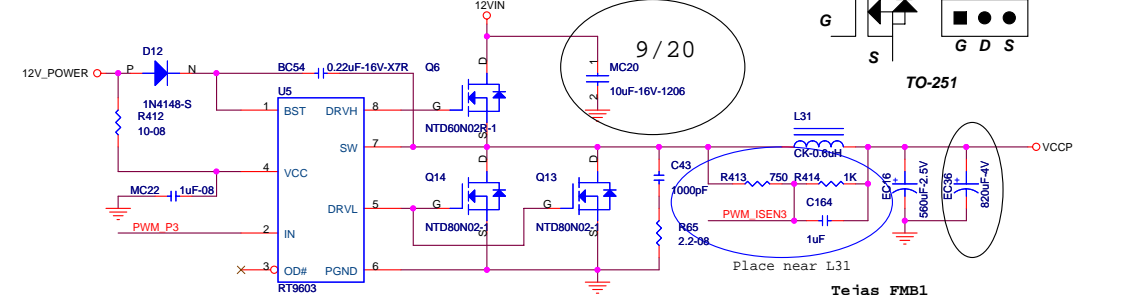
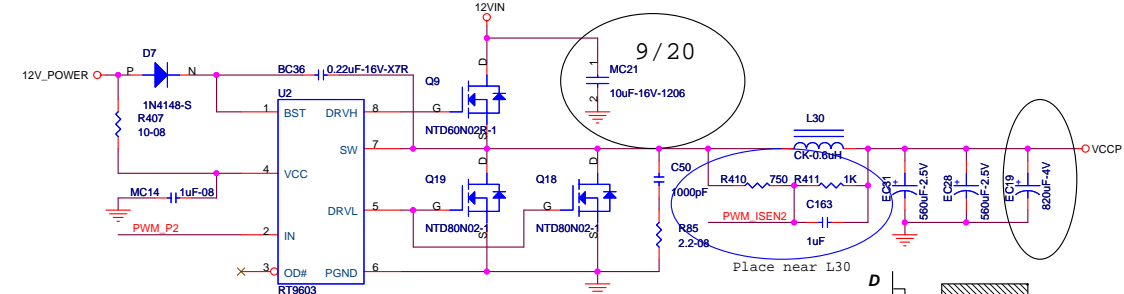
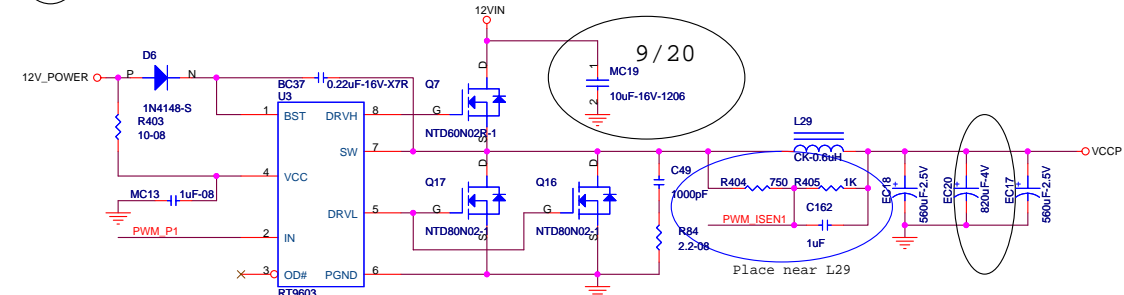
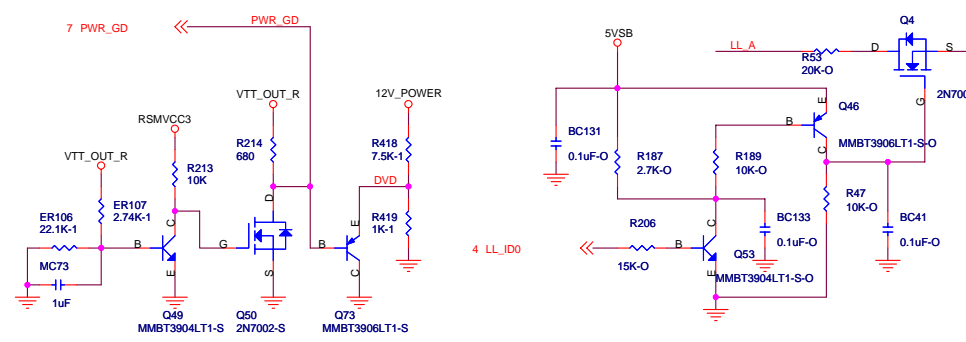
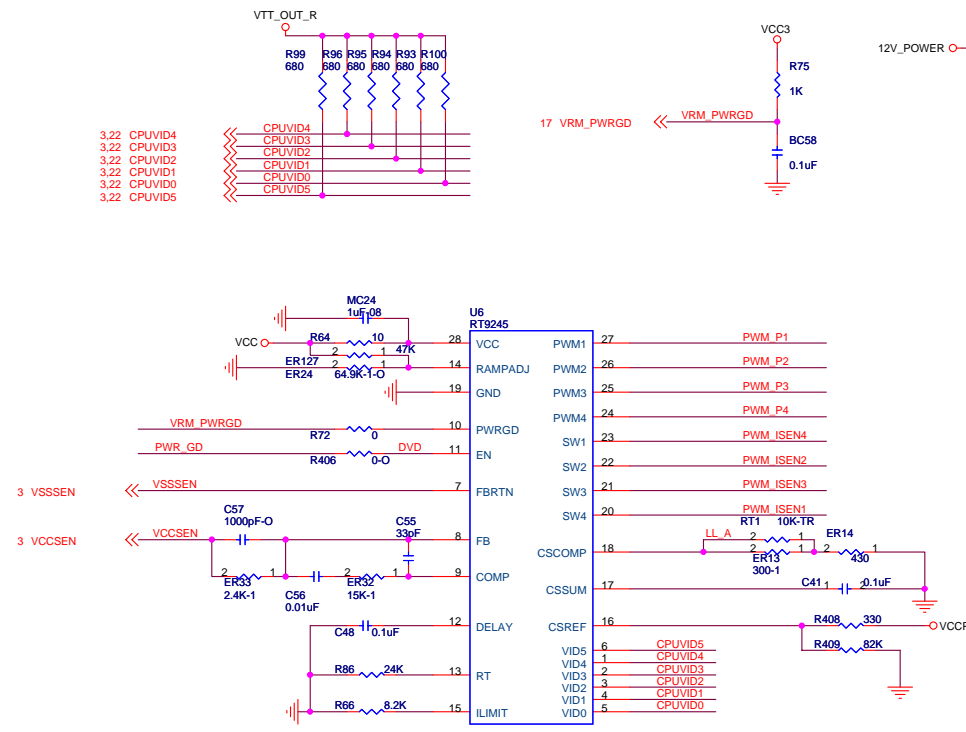
9/20

33 LINK << LINK R522 330  
33 TX\_RX << R523 330



Install only for  
RTL810S(B)  
with 93C56.



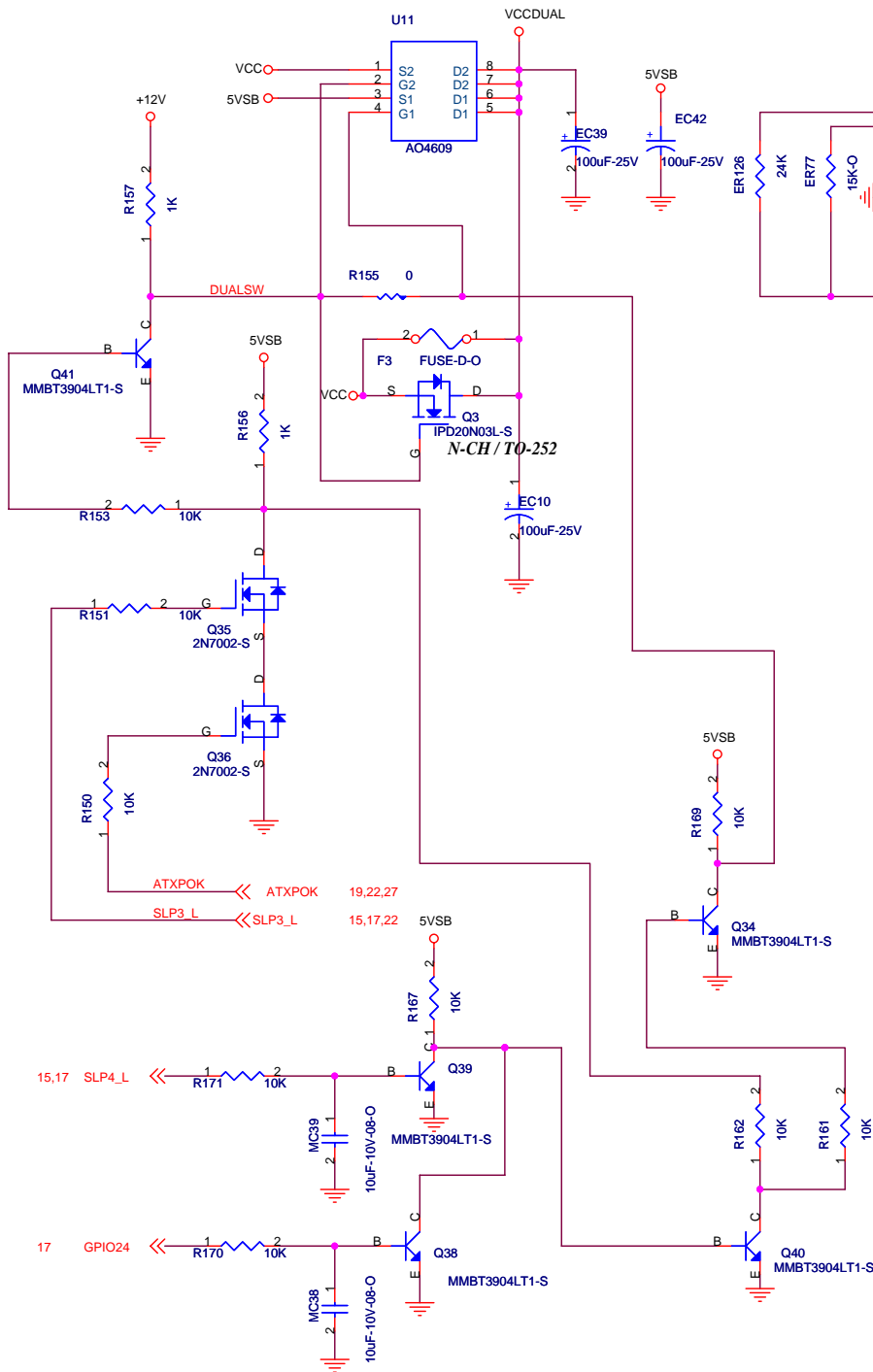


TDP POWER		Icc	MAX	Icc	TDC	Tcase
PSC=111W		119A	101A	PSC=	70 °C	
Tejas=115W				Tejas=	68 °C	

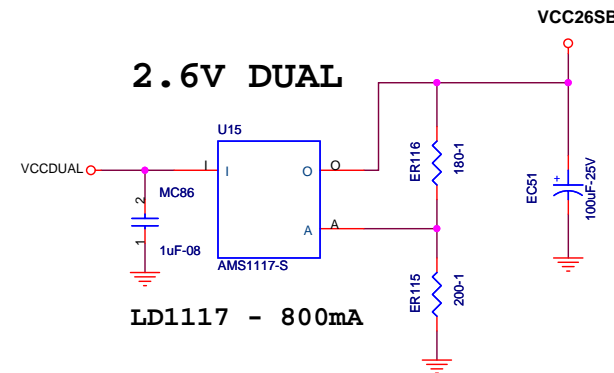
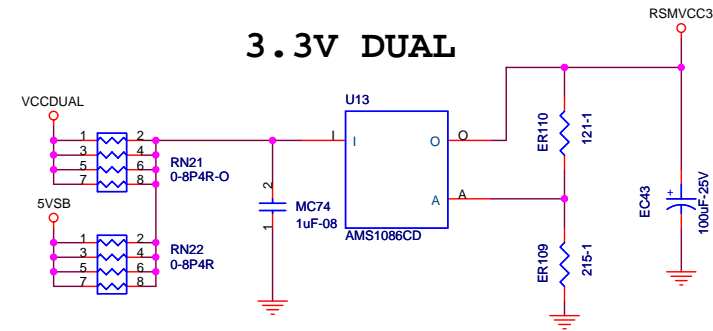
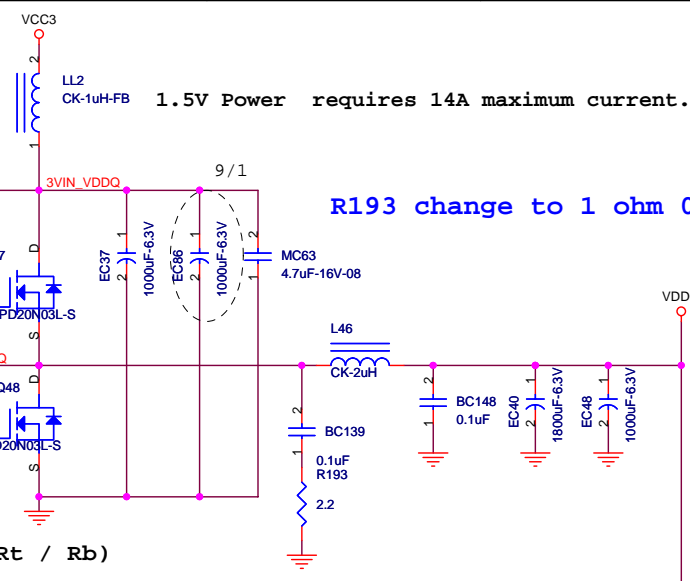
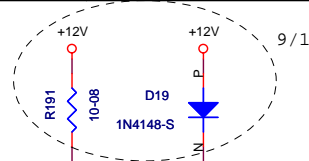
  

ECS Elitegroup Computer Systems	
Title	
VOCRE DC-DC	
Size	Document Number
Custom	915GV-M5A
Date:	Monday, April 11, 2005
Sheet	29 of 36
Rev	1.1

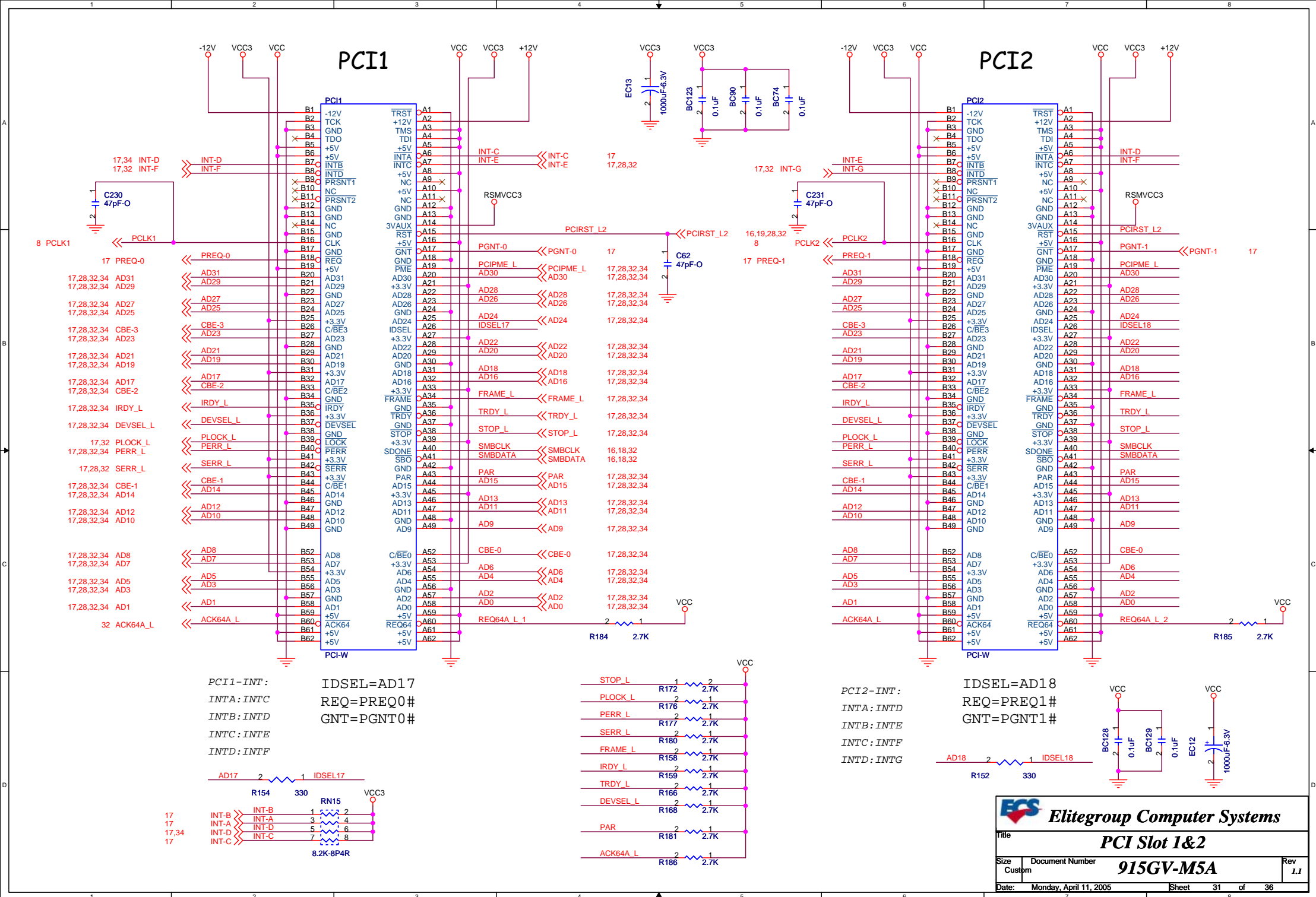
DUALSW << DUALSW 15

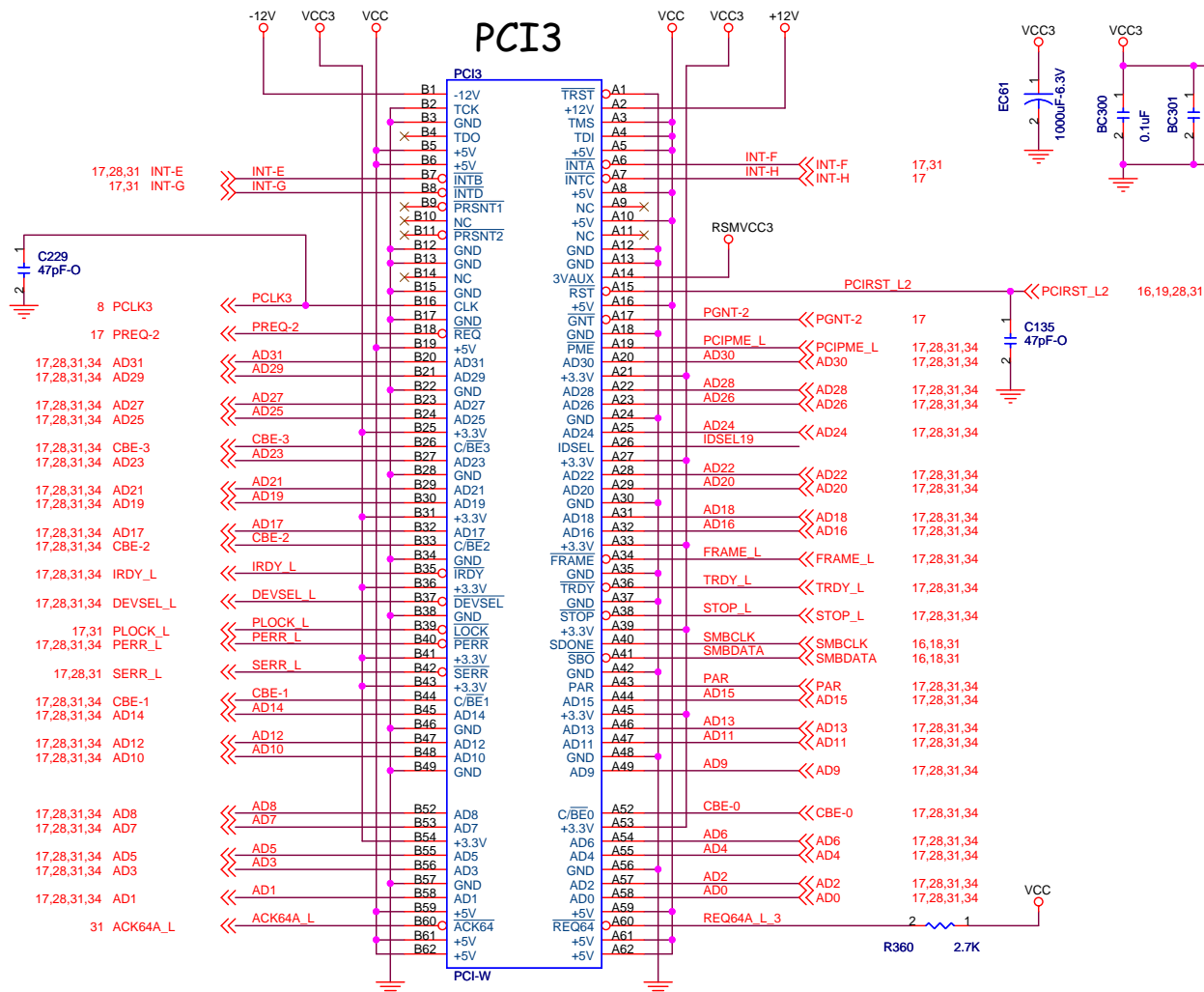


Signal Mode	GPIO24	VCCDUAL
S4/S5	0	0(No Power)
S4/S5	1	1(5VSB)

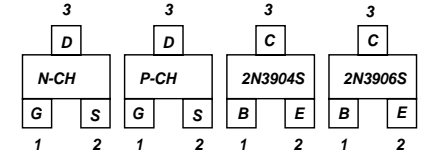
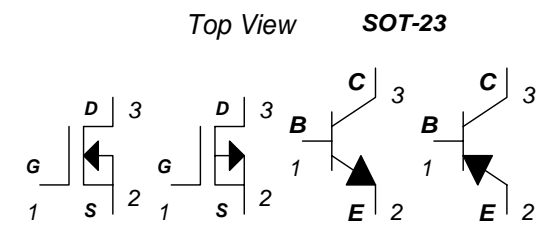
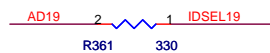


VCC26SB needs supply 570mA of current.

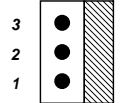




PCI3-INT: IDSEL=AD19  
 INTA: INT-E  
 INTB: INT-F  
 INTC: INT-G  
 INTD: INT-H

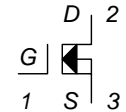


Fan Header

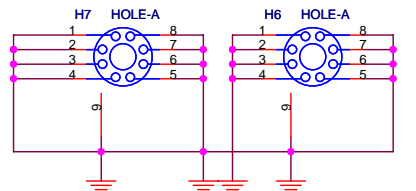
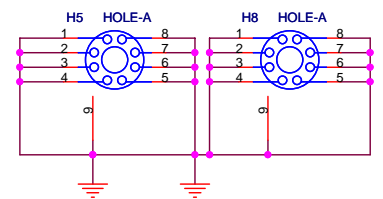
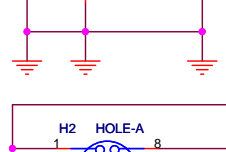
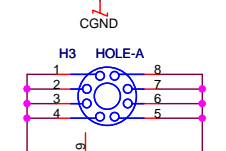
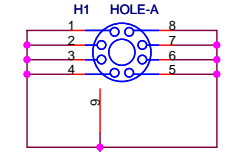
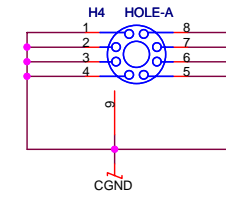
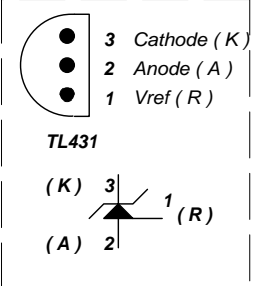


AMP640456-3

TO-263 / TO-252



Top View



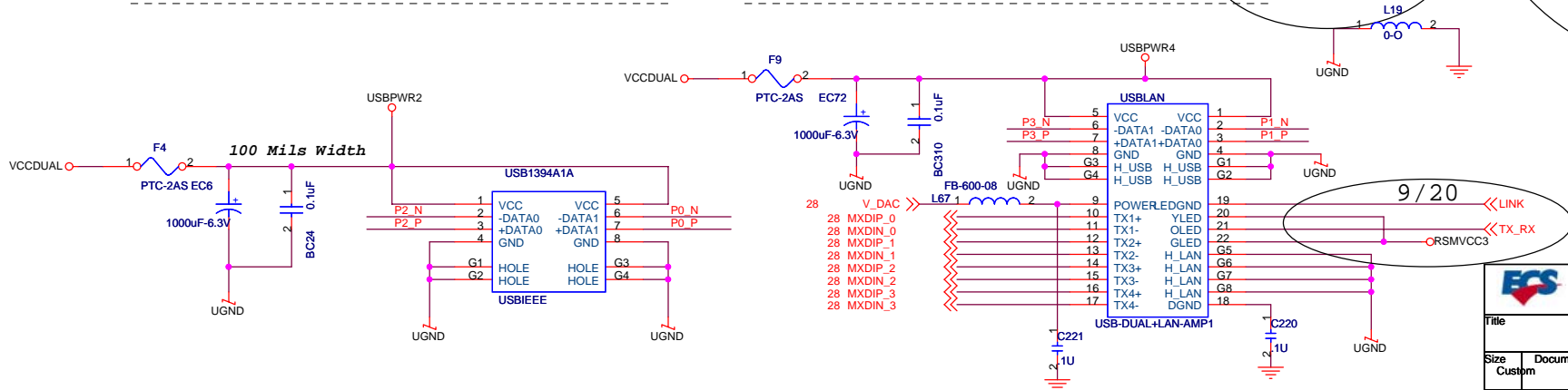
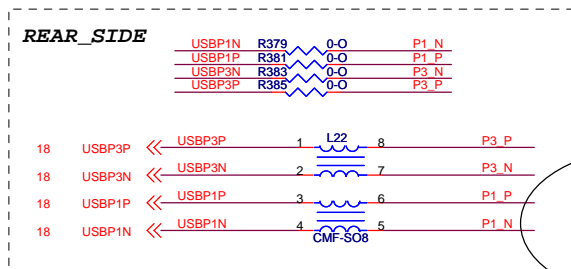
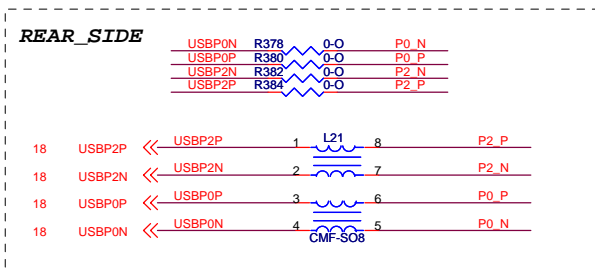
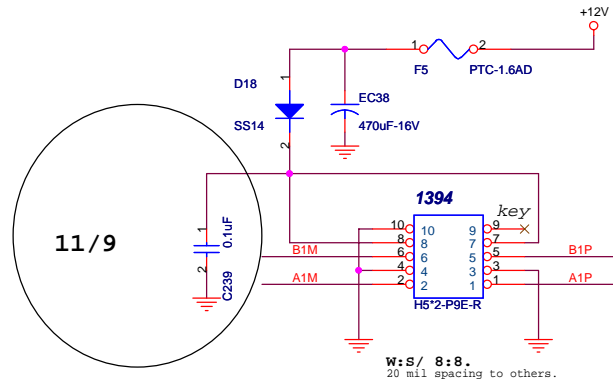
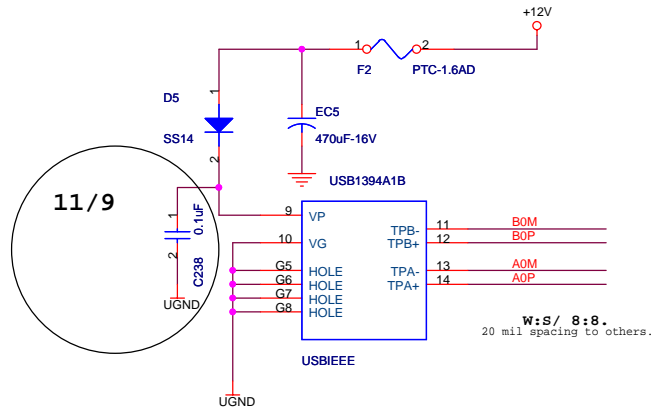
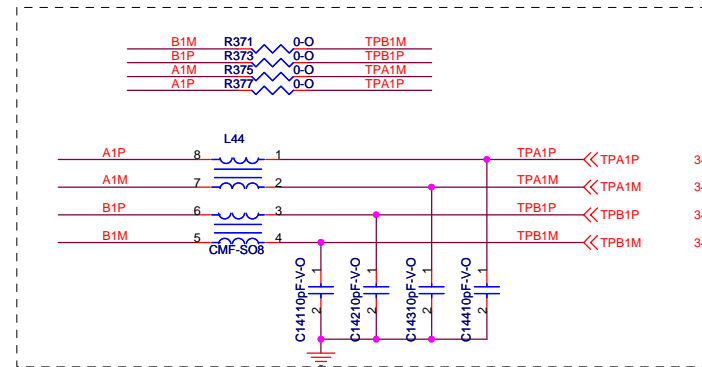
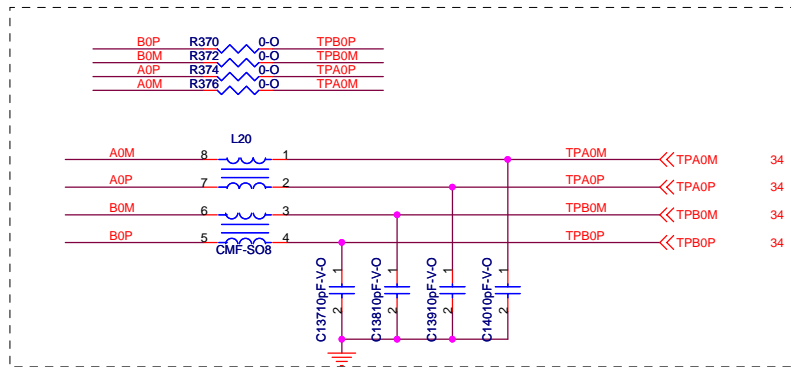
**Elitegroup Computer Systems**

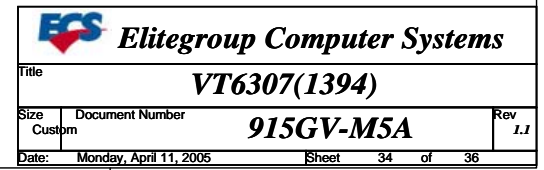
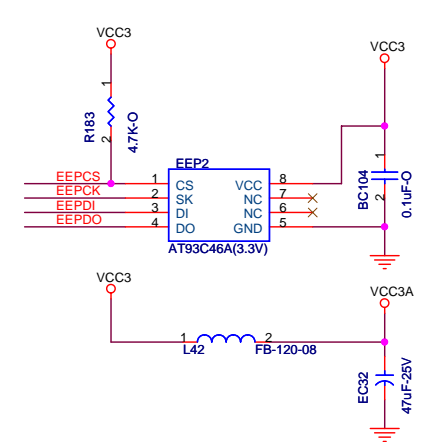
Title: **PCI Slot 3**

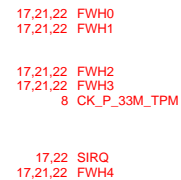
Size B Document Number: **915GV-M5A** Rev 1.1

Date: Monday, April 11, 2005 Sheet 32 of 36










1	2	3	4	5	6	7	8
A							
B							
C							
D							

 <b>Elitegroup Computer Systems</b>		
Title <b>Schematic Change History</b>		
Size Custom	Document Number <b>915GV-M5A</b>	Rev <b>1.1</b>
Date: Monday, April 11, 2005	Sheet 36 of 36	